무선 패킷 데이터를 위한 Burst switching 의 모델링 및 분석

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Modeling and Analysis of Burst Switching for Wireless Packet Data

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The third generation mobile communication needs to provide multimedia service with increased data rates. Thus an efficient allocation of radio and network resources is very important. This paper models the 'burst switching' as an efficient radio resource allocation scheme and the performance is compared to the circuit and packet switching. In burst switching, radio resource is allocated to a call for the duration of data bursts rather than an entire session or a single packet as in the case of circuit and packet switching. After a stream of data burst, if a packet does not arrive during timer2 value (τ_2), the channel of physical layer is released and the call stays in suspended state. Again if a packet does not arrive for timer1 value (τ_1) in the suspended state, the upper layer is also released. Thus the two timer values to minimize the sum of access delay and queuing delay need to be determined. In this paper, we focus on the decision of τ_2 which minimizes the access and queueing delay with the assumption that traffic arrivals follow Poison process. The simulation, however, is performed with Pareto distribution which well describes the bursty traffic. The computational results show that the delay and the packet loss probability by the burst switching is dramatically reduced compared to the packet switching.

Keyword: burst switching, wireless packet data, access delay, queueing delay, loss probability

1. Introduction

Third generation systems need to support high bit rates to provide high quality voice service as well as high-speed packet data. Thus, they need a mechanism to share the radio and network resources efficiently amongst prospective clients.

Recent traffic analyses show the inefficiency of conventional channel allocation schemes. Traditional circuit switching guarantees continuous physical and upper layer connections between the user and the network for the entirety of a session. Circuit switching is obviously inefficient for packetized data traffic where long idle periods between consecutive packets may be observed. The poor resource utilization and consequently large queuing delays and loss probability for new users in a heavy traffic system can be overcome by using packet switching instead. Packet switching, while reducing the average queuing delay and increasing the efficiency of resource utilization, introduces large average per packet access delay because every packet must access the channel.

The proposed burst switching technique aims to overcome these problems by allocating the radio resource to a user for the duration of the burst of data and releasing them at the end of the bursts for other users. Here, users would release the physical layer resources at the end of the bursts but continue to hold on to the upper layer resources provided that the inter-burst duration is small. If the inter-burst duration is

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large, upper layer resources are released as well. Therefore the decision of two timers that are used to release the physical and upper layer resource is important. Oguz et al (1999) propose a constraint in the form of a percentile of no access delay packets and suggest timer values that satisfy this constraint. Ozer et al (1999) simulate the burst switching and it is shown that for a given arrival process and QoS requirement of the users, the system parameter (timer value) of the burst switching and the required number of channels can be obtained by minimizing the access and queuing delay.

In this paper, we model each switching scheme with queuing system and determine_optimal timer2 value that minimizes the sum of access and queuing delay. With the result of modeling, we show that burst switching outperforms other switching schemes.

It is shown that the Pareto distribution well describes bursty traffic such as packet data. (M. Nabe,1997) Note that it is difficult to model the burst switching with the assumption that packet arrival follows Pareto distribution. Thus, in this paper the Poisson process is assumed to model the switching schemes. However, the simulation is preformed with Pareto distribution. The timer2 value is determined based on the result from the modeling and the simulation.

In section 2, we explain the MAC state transition in circuit, packet and burst switching schemes. The traffic model to be used for the wireless packet is described in section 3. Section 4 presents the modeling of each switching scheme. Analysis of modeling and simulation are given in section 5 with conclusion in section 6.

2. MAC State Transition for wireless packet data

2.1 Circuit and Packet Switching

When the circuit switching is employed, a dedicated connection (both physical and upper layer) is allocated to each active user for the entirety of a call. Upon the arrival of a new call, a dedicated connection is allocated to the user if there is available radio resource. If all channels are busy, the user is queued and is permitted to re-attempt the access after a uniformly distributed random delay. Media Access Control (MAC) state transitions for the circuit switching is illustrated in Figure 1-a. We assume that an access delay of τ_{a1} is observed for each dormant user for the access to the channel. Upon the completion of the session, the user goes back to the dormant state. A user in a queue is blocked if the waiting time in the queue exceeds a pre-determined tolerance time.

In the packet switching, a radio channel is allocated to users on a packet basis. After the transmission of a packet, the connection (both physical and upper layer) is released and the user becomes dormant. Subsequent packets require new access attempts to the network to obtain network resources. If all channels are busy at the time of access attempt, the user is queued and is permitted to re-attempt access after a uniformly distributed random delay. Since an access delay of τ_{a1} is observed for each dormant user, all packets in a session experience the access delay. The MAC state transition diagram for the packet switching is shown in Figure 1-b. In this paper, by assuming the same QoS for all users, the queue is established on the basis of the first come first served.

2.2 Burst Switching

The burst switching can be viewed as a visualization of the proposed MAC algorithm for CDMA2000, the North American Radio Transmission Technology (RTT) submission to the ITU. The idea is to allocate a radio channel to a user as long as the user efficiently utilizes the resource. The goal is to minimize the average observed delay per packet for users while maintaining an efficient utilization of the radio resource. In burst switching three MAC states are considered for the packet data users: active, suspended and dormant. The difference here is that the active user remains active as long as the packet inter-arrival time is shorter than a timer τ_2. If a packet inter-arrival time exceeds τ_2 for an active user, the user goes to suspended state, where the physical layer connection is released but upper layer connection is maintained. If a packet inter-arrival time again exceeds τ_1 for the user in the suspended state, the upper layer connection is released as well. The user then goes into the dormant state.

A user in the dormant state has to experience access delay of τ_{a1} to move to the active state, and a user in the suspended state has to experience access delay of τ_{a2} to go into the active state. It is considered that τ_{a2} is shorter than τ_{a1}. The MAC state transition diagram for the burst switching is given in Figure 1-c.

If all radio channels are occupied, incoming users are queued until the channels become free. Since the required QoS is assumed equal for all users, the queue is established as the first come first served queue.

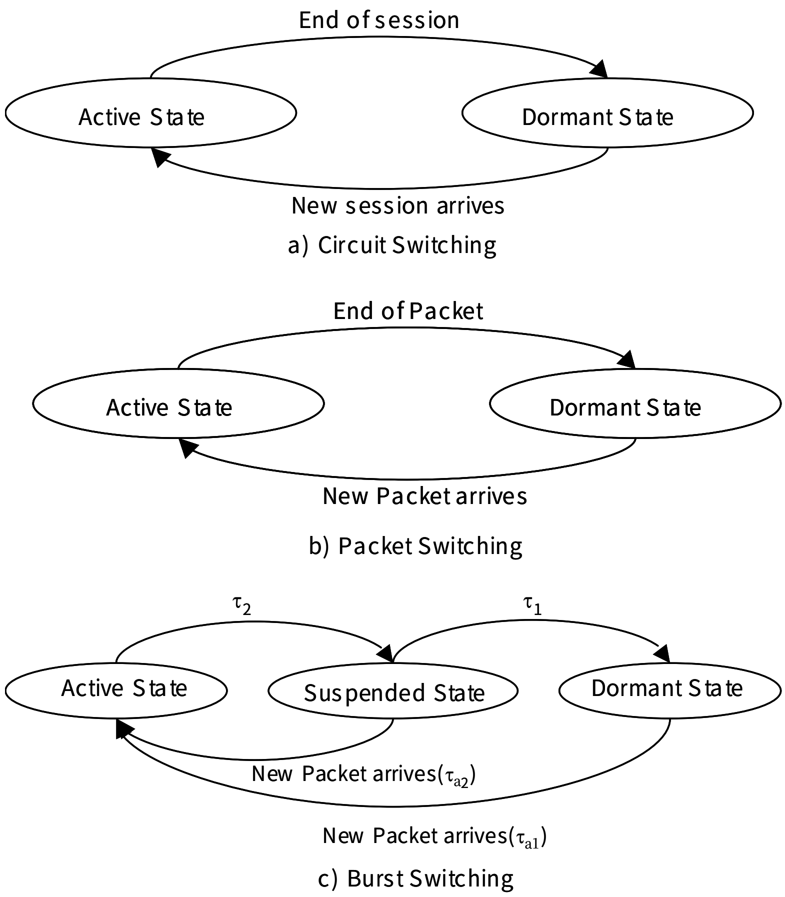


Figure 1 State diagram of switching schemes

3. Traffic Model for Wireless Packet Data

The traffic model to be discussed in this paper is depicted in Figure 2. The figure shows that a call consists of packets, and a group of packets comprises a burst, which means that a set of packets whose inter-arrival time is shorter than τ_2 makes a burst. During the burst period the user is in active state. If a packet inter-arrival time exceeds τ_2, then the user moves to suspended state, since the burst of packets is stopped temporarily.

We assume that calls arrive with Poisson process with arrival rate λ_u and the session durations are exponentially distributed with parameter μ. Session durations are independent each other, also they are independent of the packet inter-arrival times.

The call arrival rate λ_u is independent of the packet arrival rate λ_p. The session duration is also independent with packet transmission time.

It is well known that packet inter-arrival times within a session are distributed according to a Pareto distribution with shape parameter α and location parameter k which dictates the minimum inter-arrival time. (Oguz, M., 1999)

$$P(t \le \varphi) = 1 - \left(\frac{k}{\varphi}\right)^{\alpha}, \quad k, \alpha \ge 0, \varphi \ge k \tag{1}$$

Note that it is difficult to model switching schemes with Pareto distributed packet inter-arrival times. Thus, we model each switching scheme with assumption that packets arrive in Poisson process with the arrival rate of λ_p. However, the simulation of burst switching is performed with Pareto distributed packet inter-arrival times.

In CDMA2000 wireless packet system, data is transmitted through frames each with 20ms. Since the maximum length of IP packet is 2^{16} bytes and the maximum data rate is 0.643Mbps, it takes about 0.8 second (40frames) to transmit the longest packet. Accordingly, we assume that the packet transmission time (t_t) follows discrete uniform distribution in the interval (0.02, 0.8). Note that the expected value of packet transmission time, $E(t_t)$ is 0.41 second, and $E(t_t^2)$ is 0.05.

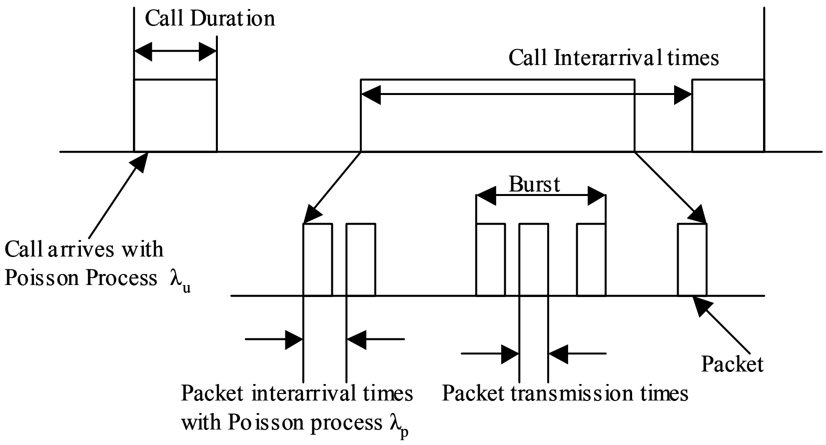


Figure 2 Traffic Model

4. Modeling of the Switching System

We model each switching scheme with queueing systems and determine optimal timer2 ($\tau 2$) value that minimizes the sum of access and queueing delay under the assumption that the burst switching has an infinite queue. In the real system, however, the buffer is finite. Thus the optimal timer2 value has to be determined such that the delay is minimized. By assuming the infinite buffer in the burst switching, the system model can provide the worst case delay of the real system. The infinite buffer also guarantees minimized packet loss probability. For the worst case packet loss probability, we additionally derive packet loss probability for the system without buffer.

4.1 Circuit Switching

The circuit switching is modeled as M/M/C/∞. The input parameters are call arrival rate, λ_u and the output rate, μ. Traffic load, ρ is λ_u /Cμ. As the well known waiting time formulation for M/M/C, the queuing delay per call in circuit switching is

$$T_{Q\_Call} = \frac{C_e \rho}{\lambda(1-\rho)} \quad = \frac{P_c}{(1-\rho)2} \frac{1}{\mu} \tag{2}$$

where C_e is *Erlang C formula* as in (3) and P_i denotes the probability that the number of customers in the systems is *i*.

$$C_e = P(N \geq C) = \sum_{n=c}^{\infty} P_n = P_c / (1-\rho) \tag{3}$$

To compare the queueing delay of circuit switching with that of packet switching, the queuing delay per packet T^C_{QUEUE} is divided by the expected number of packets in a session, N_p. Thus, the average packet delay of circuit switching is given by

$$T^C_{QUEUE} = T_{Q\_Call} / Np. \tag{4}$$

An access delay of τ_{a1} is observed for each dormant user to access to the channel. In circuit switching, an access delay of τ_{a1} is observed only for the first packet in a session. The expected access delay for a packet is equal to τ_{a1} divided by the expected number of packets in a session.

$$T^C_{ACCESS} = \tau_{a1}/Np \tag{5}$$

Additionally, we find the loss probability for the system without buffer. The loss probability is given by Erlang B Formula, as in (6).

$$P_c = \frac{(\lambda/\mu)^c}{c!} P_0, \quad P_0 = [\sum_{n=0}^{c} \frac{(\lambda/\mu)^n}{n!}]^{-1} \tag{6}$$

Thus the loss probability of circuit switching is

$$P_c = \frac{(\lambda_u/\mu)^c}{c!} P_0 \ , \ P_0 = [\sum_{n=0}^{c} \frac{(\lambda_u/\mu)^n}{n!}]^{-1} . \tag{7}$$

4.2 Packet Switching

In the packet switching, radio resources are allocated to calls on a packet basis. Thus, we model packet switching for a unit of packet. If there are N calls in the system and each call generates packets with rate λ_p, the aggregate packet arrival process becomes a Poisson process with arrival rate $N\lambda_p$.

We model the packet switching as M/G/C/∞ with input rate $N\lambda_p$ and output rate $1/E(t_t)$. The queuing delay per packet in the packet switching is given by the well known approximation of the waiting time for M/G/s queue.

$$T^{P}_{QUEUE} = \frac{E(t_{tR}')}{(1-\rho_{packet})} C_e \tag{8}$$

The load of packet switching, ρ_{packet} is $N\lambda_p E(t_t)/C$. t_{tR}' is the remaining time of t_t/C.

$$E(t_{tR}') = \frac{E(t_t^{\,2})}{2E(t_t)C} \tag{9}$$

In packet switching, an access delay of τ_{a1} is observed for every packet in a session. Thus, the access delay per packet is given by

$$T^{P}_{ACCESS} = \tau_{a1}. \tag{10}$$

Additionally, the loss probability for the packet switching without buffer is given as follows by the Erlang B Formula.

$$P_c = \frac{(N\lambda_p E(t_t))^c}{c!} P_0, \quad P_0 = [\sum_{n=0}^{c} \frac{(N\lambda_p E(t_t))^n}{n!}]^{-1} \tag{11}$$

4.3 Burst Switching

In the burst switching, a call is allocated to a channel upon the arrival of a new packet. The access delay is τ_{a1} if there is an available radio channel. The call state moves to active state from dormant state. The call remains active as long as the packet inter-arrival times are shorter than a timer, τ_2. If a packet inter-arrival time exceeds τ_2 for an active call, the state of the call moves to the suspended state. A user in the suspended state releases the physical layer connection, but maintains upper layer connections. Once the user is in the suspended state, the next burst experiences access delay of τ_{a2}. Packets in the burst do not experience any access delay, however, may experience a queueing delay.

We assume the system has C channels and N calls. Let λ_{burst} be the burst arrival rate and N_{burst} be the expected number of packets within one burst. Then the input rate to the system becomes $N\lambda_{burst}$. λ_{burst} is λ_p divided by $E(N_{burst})$.

$$\lambda_{burst} = \lambda_p / E(N_{burst}) = \lambda_p e^{-\lambda_p \tau_2} \tag{12}$$

$$N\lambda_{burst} = N\lambda_p e^{-\lambda_p \tau_2} \tag{13}$$

The output rate is 1/(the duration that a channel is occupied by a burst). We denote the duration that a channel is occupied by a burst with BP (Busy Period). If X(i) is the packet inter-arrival time between the i th and (i+1) th packets within a burst, then

$$BP = X(1)+X(2)+\cdots+X(N_{burst}-1) + \tau_2 = Y + \tau_2 \tag{14}$$

where, Y denotes $X(1) + X(2) + \cdots + X(N_{burst} - 1)$. As it is independent random sum, E(Y) and $E(Y^2)$ is expressed as

$$E(Y) = [E(N_{burst}-1)][E(X|X<\tau_2)] \tag{15}$$

$$E(Y^2) = E(N_{burst}-1)\, E(X^2|X<\tau_2) + [\{E(X|X<\tau_2)\}^2][E\{(N_{burst}-1)^2 - (N_{burst}-1)\}] \tag{16}$$

N_{burst} is the number of intervals of packets until inter-arrival time is greater than τ_2. N_{burst} is geometrically distributed with parameter $p=\exp(-\lambda_p\tau_2)$. $E(N_{burst})$ and $E(N_{burst}^2)$ is expressed as follows.

$$E(N_{burst}) = \frac{1}{p} = \frac{1}{\exp(-\lambda_p\tau_2)} \tag{17}$$

$$E(N_{burst}^2)=\frac{(2-p)}{p^2} = \frac{[2-\exp(-\lambda_p\tau_2)]}{[\exp(-\lambda_p\tau_2)]^2} \tag{18}$$

Thus, we have

$$E(N_{burst}-1) = \frac{1}{\exp(-\lambda_p\tau_2)} -1, \tag{19}$$

$$E[(N_{burst}-1)^2] = \frac{(1-p)(2-p)}{p^2} = \frac{(1-\exp(-\lambda_p\tau_2)(2-\exp(-\lambda_p\tau_2))}{\exp(-\lambda_p\tau_2)^2}. \tag{20}$$

Note that

$$\begin{aligned} E(X|X<\tau_2) &= \int_0^{\tau_2} Xf(X \mid X<\tau_2)dX = \int_0^{\tau_2} X \frac{\lambda_p \exp(-\lambda_p X)}{1-\exp(-\lambda_p\tau_2)}dX \\ &= \frac{1}{1-\exp(-\lambda_p\tau_2)}[\frac{1}{\lambda_p} - \tau_2\exp(-\lambda_p\tau_2) - \frac{1}{\lambda_p\exp(-\lambda_p\tau_2)}], \end{aligned} \tag{21}$$

$$E(X^2|X<\tau_2) = \int_0^{\tau_2} X^2 f(X \mid X < \tau_2) dX = \int_0^{\tau_2} X^2 \frac{\lambda_p \exp(-\lambda_p X)}{1-\exp(-\lambda_p \tau_2)} dX$$

$$= \frac{1}{1-\exp(-\lambda_p \tau_2)} \left[\frac{2}{\lambda_p{}^2} - \exp(-\lambda_p \tau_2) \left\{ \tau_2{}^2 + \frac{2\tau_2}{\lambda_p} + \frac{2}{\lambda_p{}^2} \right\} \right]$$

$$= \frac{2}{\lambda_p{}^2} - \frac{\tau_2 \exp(-\lambda_p \tau_2)}{1-\exp(-\lambda_p \tau_2)} \left[\tau_2 + \frac{2}{\lambda_p} \right]. \tag{22}$$

Thus E(Y) and E(Y^2) can be obtained from equations (15) ~ (22).
Note that E(BP) and E(BP^2) are given by

$$E(BP) = E(Y) + \tau_2 \tag{23}$$

$$E(BP^2) = E(Y^2) + 2\tau_2 E(Y) + \tau_2{}^2 \tag{24}$$

The output rate is 1/E(BP).

The queuing delay per burst is given by an approximation for the waiting time for M/G/s queue.

$$T_{Q\_Burst} = \frac{E[BP_R']}{(1-\rho_{burst})} C_e \tag{25}$$

The load of burst switching, ρ_{burst} is $N\lambda_{burst}E(BP)/C$. We denote BP' as BP/C, then we have

$$E(BP_R') = \frac{E(BP^2)}{2E(BP)C}. \tag{26}$$

The queuing delay per packet becomes

$$T^B_{QUEUE} = T_{Q\_Burst} / N_{burst} \tag{27}$$

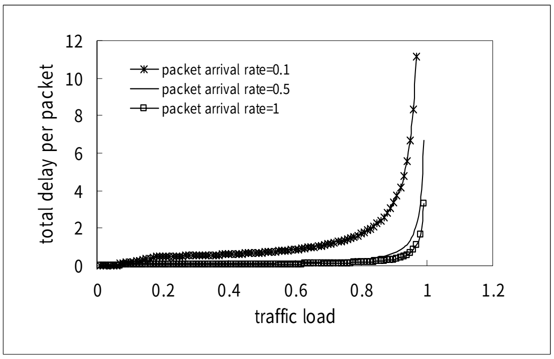
Note that if the packet inter-arrival time is less than τ_2, the packet does not experience any access delay. If the inter-arrival time is between τ_1 and τ_2, the packet experiences access delay τ_{a2}. Also, if the packet inter-arrival time is greater than τ_1, the access delay becomes τ_{a1}.

Thus, the mean value of access delay of a packet (except the initial packet) is:

$$T^B{}_{ACCESS} = [\exp(-\lambda_p \tau_1)]\tau_{a1} + [\exp(-\lambda_p \tau_2) - \exp(-\lambda_p \tau_1)]\tau_{a2} \tag{28}$$

Additionally, we compute the loss probability for the system without buffer as

$$P_c = \frac{(N\lambda_{burst}E(BP))^c}{c!} P_0, \quad P_0 = [\sum_{n=0}^{c} \frac{(N\lambda_{burst}E(BP))^n}{n!}]^{-1} \tag{29}$$



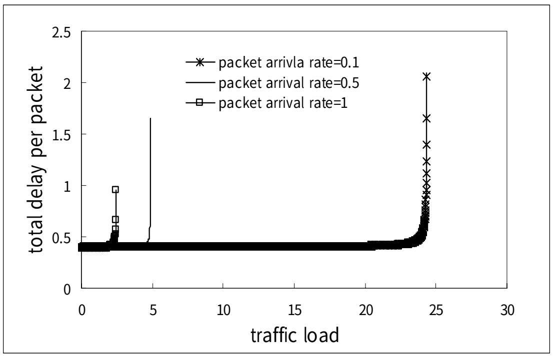


Figure 3 Computational result of Circuit Switching Model

Figure 4 Computational result of Packet Switching Model

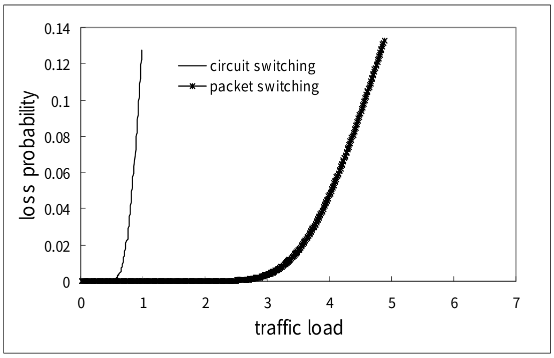


Figure 5 Loss probability of circuit and packet switching

5. Analysis of the Modeling and Simulation

In this section, we assume that the traffic model has the parameters C=30, μ=1/600, τ_1=15, τ_{a1}=0.4, and τ_{a2}=0.2. τ_1 is fixed throughout the experiments because it has little effect on the performance of the system compared to τ_2. Moreover, it should be noted that τ_{a2} is shorter than τ_{a1}.

5.1 Circuit and Packet switching

The analysis in section 4.1 for the circuit switching is illustrated in Figure 3. The figure shows total delay as a function of the traffic load for different packet arrival rates λ_p = 0.1, 0.5, and 1.0. As the traffic load ($\rho=\lambda_u$ / Cμ) converges to 1, total delay diverges explosively. The figure shows that for increased packet arrival rate, total delay per packet decreases, which means better utility. It is clear that increasing the packet arrival rate means reducing the idle period between consecutive packets while in the active states. Therefore when λ_p is increased, the circuit switching has better utility.

The result in section 4.2 for the packet switching is illustrated in Figure 4. In the figure we observe that for low traffic load (less than 1.31 for λ_p = 0.1, less than 0.27 for λ_p = 0.5 and less than 0.14 for λ_p = 1), the total delay per packet does not change with increased traffic load. This is due to the fact that for

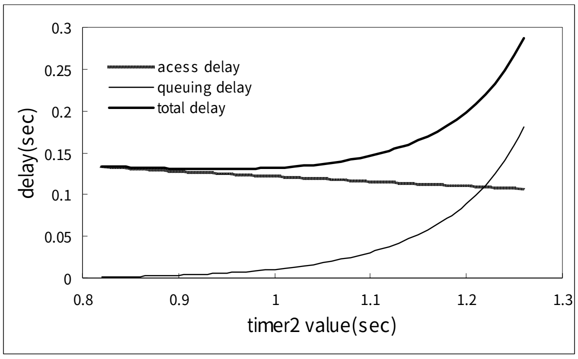


Figure 6 Computational result of Burst Switching Model

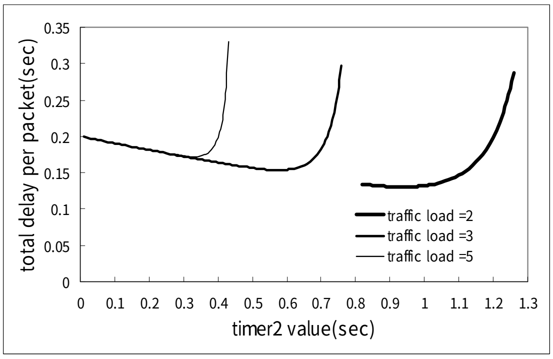


Figure 7 Timer2 values of Burst Switching for different traffic load

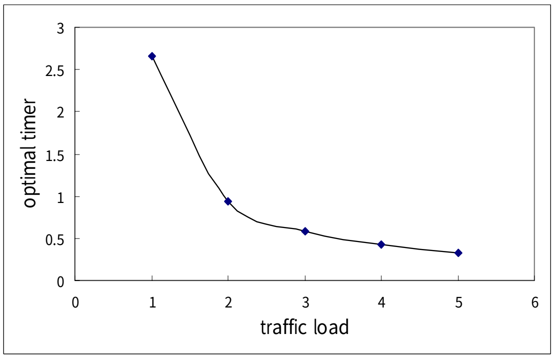


Figure 8 Optimal timer value of Burst Switching

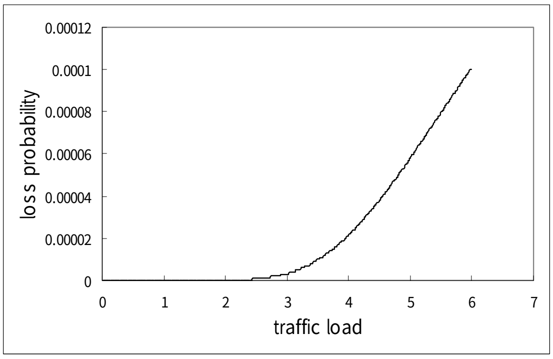


Figure 9 Loss probability of burst switching

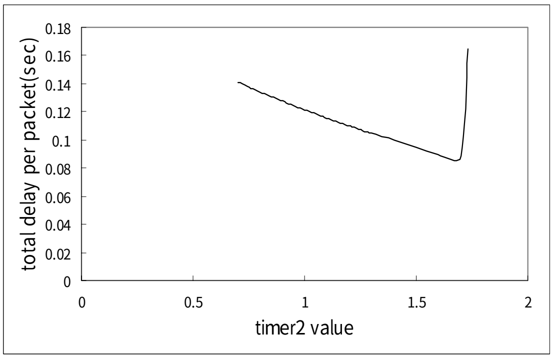


Figure 10 Simulation result for traffic load=2

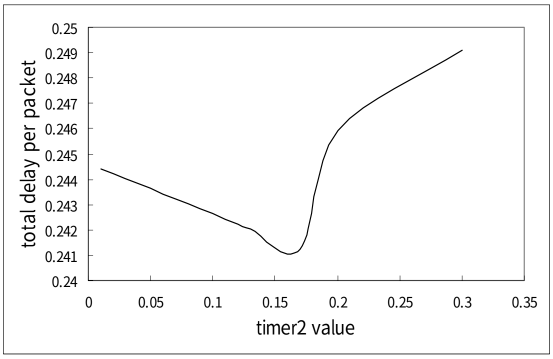


Figure 11 Simulation result for traffic load=5

the low traffic load, the system has enough radio channels for packet switching and no user experiences queuing delays.

The figure shows total delay diverges as traffic load converges to 24.39 for $\lambda_p = 0.1$, 4.87 for $\lambda_p = 0.5$, and 2.43 for $\lambda_p = 1$. Note that the above traffic loads corresponds to the traffic load in circuit switching from which ρ_{packet} can be derived. The arrival rate of packets is $N\lambda_p$ and output rate is $E(t_t)$. Since the packet switching is modeled as M/G/C/∞, N corresponds to λ_u / μ . Thus ρ_{packet} is expressed as

$$\rho_{packet} = \frac{\lambda_u \lambda_p E(t_t)}{\mu C} = \rho \lambda_p E(t_t) . \tag{30}$$

Traffics loads of 24.39, 4.87, and 2.43 are values that make ρ_{packet} = 1. It means that the packet switching can accommodate much more users than the circuit switching, i.e., transmission efficiency of the packet switching is superior to that of the circuit switching. However, in low traffic load, total delay of the packet switching is larger than that of the circuit switching because of the frequent access delay of the packet switching.

From the result of the circuit and the packet switching, we expect that the optimal timer2 value for the burst switching can be expressed as a function of the traffic load, ρ and packet arrival rate, λ_p.

Figure 3 and 4 show that when the traffic volume is low, the circuit switching gives better performance. But for heavy traffic, the packet switching outperforms the circuit switching. In the packet switching, access delay is larger than queuing delay since every packet in a session accesses the channel. On the other hand, in circuit switching, access delay per packet is negligible because only the first packet in a session takes access delay. However the queuing delay is noticeable due to the dedicated channel until a call is terminated.

The analysis also shows the access delay more affects total delay when there is not much traffic load. But when the traffic load is heavy, queuing delay has a bigger effect on total delay.

Figure 5 shows the loss probability of circuit and packet switching without buffer. Clearly, low loss probability is kept with increased traffic load in the packet switching.

5.2 Burst Switching

The result of the analysis in section 4.3 is plotted in Figure 6, 7, 8, and 9. Since the results for different value of λ_p have the similar trend, we show the case of λ_p =0.5. Note that

$$\rho_{burst} = \frac{N\lambda_{burst} E(BP)}{C} = \rho \lambda_p e^{-\lambda_p \tau_2} < 1 . \tag{31}$$

Figure 6 shows access delay, queuing delay and total delay as a function of the timer value for ρ = 2. The figure shows that the access delay decreases and the queuing delay increases as the value of timer2 increases. Note that as the value of timer2 increases, the probability that the packet experiences access delay increases. Thus, the access delay per packet increases. On the other hand, as the value of timer2 increases, the idle period during active state increases and the channel utility decreases. Thus queuing delay increases. The total delay decreases for timer value τ_2 < 1.0 and increases for values of τ_2 > 1.0. For τ_2 = 1.0, total delay is minimized and the delay is 0.13203sec. Thus τ_2 = 1.0 is the optimal timer2 value for ρ = 2.

The computational result of the burst switching for different traffic loads ρ = 2, 3, and 5 is illustrated in Figure 7. The packet delay is minimized at τ_2 = 1.0, 0.58, and 0.33 seconds for traffic load ρ = 2, 3, and 5 respectively. Note that as traffic load increases, the queuing delay increases and the idle channels have to be released for bursts. Thus, the optimal timer2 value becomes smaller as the traffic load increases.

Figure 8 shows optimal value of timer2 for different traffic load. It shows that optimal timer2 value decreases as traffic load increases. For heavy traffic, note that the queuing delay affects the total delay more than the access delay. To reduce queuing delay, timer2 value must be decreased so that other bursts can access the channel.

Figure 9 shows the loss probability of burst switching. Compared to the loss in the packet and circuit switching, the loss probability is dramatically reduced by the burst switching. The increase of loss seems to be linear to the traffic load.

The simulation result of total delay per packet for burst switching is illustrated in Figure 10 and 11. Compared to the analysis from modeling, the optimal timer2 value from the simulation is larger in low traffic and smaller in high traffic load. This seems to be due to the burstiness of Pareto distribution used in simulation.

6. Conclusion

This paper discusses the modeling and performance of the circuit, packet and burst switching. Computational results show that the burst switching gives the best performance both in packet loss and delay. In a system without buffer, the burst switching shows the lowest loss probability. Also in a system with buffer, the packet delay is minimized by the burst switching.

The packet delay in the burst switching is expressed as a function of timer2 value, packet arrival rate and traffic load. The optimal timer2 values that minimize the packet delay for different traffic load are obtained from the computational result. The experimental analysis shows that the optimal timer2 value decreases as the traffic load increases.

References

Huebner, F., Liu, D., and Fernandez, J. M. (1998), Queuing Performance Comparison of Traffic Models for Internet Traffic, IEEE GLOBECOM 1998.

Nabe, M., Murata, M., and H. Miyahara (1997), Analysis and Modeling of WWW Traffic for Capacity Dimensioning for Internet Access Lines, Proceeding of SPIE Conference on Performance and Control of Network Systems, Dallas, November 1997.

Oguz, M., Tekinay, S., and Ozer, S. Z. (1999), Efficient Allocation of Radio Resource for CDMA Based Wireless Packet Data systems, GLOBECOM 1999 638-643.

Ozer, S. Z. (1999), Burst Switching For Third Generation Wireless Communications, VTC 1999.

Schwartz, M. (1996), Broadband Integrated Network, Prentice Hall 75-79.

So, J. W. and Cho, D. H. (2000), On Effect of timer object for Sleep Mode Operation in CDMA2000 System, IEEE 2000.

Stallings, W. (1998), High-Speed Networks, TCP/IP And ATM Design Principles, Prentice Hall 181-207.

Telecommunications Industry Association (1998), The cdma2000 ITU-RTT Candidate Submission-TR45-5.5, submission to ITU.

Willinger, W., Taqqu, M. S., and Erramilli, A. (1996), A bibliographical guide to self-similar traffic and performance modeling for modern high-speed networks, Stochastic Networks: Theory and Applications, Clarendon Press, Oxford 339-366.